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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/069,352	08/07/2002	Gilbert Wolrich	10559-308US1	7931

20985 7590 02/24/2006

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EXAMINER	
HUISMAN, DAVID J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 02/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/069,352	WOLRICH ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-38 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Change of Address as received on 10/13/2005 and Amendment as received on 12/2/2005.

Non-Compliance

3. Applicant has failed to comply with revised 37 CFR 1.121, which is required as of July 30, 2003, and 37 CFR 1.72. More specifically, applicant's amended abstract must appear on a separate sheet of paper.

Specification

4. The disclosure is objected to because of the following informalities:

* In the amended paragraph beginning on page 10, line 27, replace "symbolic names that of the corresponding CSRs" with -- symbolic names of the corresponding CSRs-- On page 3, line 9, replace "16b" with --26b--.

Appropriate correction is required.

Drawings

5. Applicant's amended drawings have been noted by the examiner. However, it is unclear why applicant has filed a new set of drawings which do not include the amendments. It is asked that applicant now submit formal drawings for those figures including the amendments. For instance, Fig.1 and Fig.3 fail to include applicant's amendments.

Claim Objections

6. Claim 7 is objected to because of the following informalities: In the last link, please remove "breakpoint". Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-6, 8-10, 20-25, and 27-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Nguyen, U.S. Patent No. 6,058,465 (as disclosed by applicant).

9. Referring to claim 1, Nguyen has taught a method of operating a processor comprising receiving data in a processing thread having a processing thread number and loading the data into selected bits of a register according to the processing thread number. See columns 91-92,

and note the VCHGCR instruction which is executed by one of multiple threads (column 4, lines 33-36). If multiple threads exist, then there exists a first thread, second thread, etc (they are numbered). Note from columns 91-92 that data is loaded into the VCSR register (in the CBANK, SMM, and CEM bits). For data to be loaded, it must first be received. For instance, in order to clear a bit, a 0 must be received. In order to set a bit, a 1 must be received. Since the instruction is executed by a thread, everything involved with the instruction corresponds to that particular thread.

10. Referring to claim 2, Nguyen has taught a method as described in claim 1. Nguyen has further taught that the register is a control and status register. See columns 91-92 and note that the register is a control register with status bits which dictate operation.

11. Referring to claim 3, Nguyen has taught a method as described in claim 2. Nguyen has further taught that the control and status register is coupled to a 64-bit wide first-in first-out (FIFO) bus. See Fig.1, and note the 64-bit bus coupled to component 158 which is further coupled to the rest of the system. The bus is inherently FIFO because data that is sent over the bus at time A will arrive at its destination before data that is sent over the bus at time B (where B > A).

12. Referring to claim 4, Nguyen has taught a method as described in claim 3. Nguyen has further taught that the FIFO bus interfaces with Media Access Controller (MAC) Devices. See column 1, lines 36-40 and note that the invention is concerned with multimedia applications. Therefore, it would be coupled to a media access controller.

13. Referring to claim 5, Nguyen has taught a method as described in claim 1. Nguyen has further taught that the data represents hexadecimal mask values 0 to 0x3FF. Note from columns

91-92 that the data written to the register may be either 0 (when clearing a bit) or 1 (when setting a bit). Consequently, the data represents values in the range 0 to 3FF.

14. Referring to claim 6, Nguyen has taught a method as described in claim 1. Nguyen has further taught that the processing thread represents processing in a micro engine of a multithreaded processor. Again, see column 4, lines 33-36.

15. Referring to claim 8, Nguyen has taught a method as described in claim 1. Nguyen has further taught that receiving the data further comprises receiving a token. See columns 91-92 and note that receiving the data to be written to the control register must be preceded by receiving the VCHGCR instruction (token). Therefore, the receiving of the data is coupled with receiving the token.

16. Referring to claim 9, Nguyen has taught a method as described in claim 8. Nguyen has further taught that the token represents overriding qualifiers. Since the instruction writes to a control register using the data provided in the instruction, the data represents overriding qualifiers as everything already in the control register will be overridden by new data to be written.

17. Referring to claim 10, Nguyen has taught a method as described in claim 8. Nguyen has further taught that the token is a 32-bit word. See columns 91-92 and note the instruction (token) is 32 bits.

18. Referring to claims 20-25 and 27-29, claims 20-25 and 27-29 are rejected for the same reasons set forth in the rejection of claims 1-6 and 8-10, respectively, because Nguyen has taught instructions stored on a medium for performing the method of claims 1-6 and 8-10.

19. Claims 1-6, 8-9, 20-25, and 27-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Intel, "IA-64 Application Developer's Architecture Guide," May 1999 (herein referred to as Intel).

20. Referring to claim 1, Intel has taught a method of operating a processor comprising:

a) receiving data in a processing thread having a processing thread number. See page 2-3, section 2.4 and note that multiple threads may be executed. A given thread may include a shift instruction (page 7-165) in which shifted data is obtained. Note that the thread which includes this instruction would include a thread number (shift amount).

b) loading the data into selected bits of a register according to the processing thread number. From page 7-165, the shifted data is stored in a specified register which corresponds to the thread number (shift amount). More specifically, every item (destination, source, shift amount, opcode, predicate) in the shift left instruction corresponds to one another.

21. Referring to claim 2, Intel has taught a method as described in claim 1. Intel has further taught that the register is a control and status register. Any register that is written to is a control/status register because when it is used in any future instruction as a source, it controls the outcome of that instruction.

22. Referring to claim 3, Intel has taught a method as described in claim 2. Intel has further taught that the control and status register is coupled to a 64-bit wide first-in first-out (FIFO) bus. See page 3-1 and note that the general purpose registers (which the shift left instruction operates on) are 64 bits wide. Consequently, 64-bit data must be able to be written to the register and therefore, a 64-bit bus exists. The bus is inherently FIFO because data that is sent over the bus at time A will arrive at its destination before data that is sent over the bus at time B (where B > A).

23. Referring to claim 4, Intel has taught a method as described in claim 3. Intel has further taught that the FIFO bus interfaces with Media Access Controller (MAC) Devices. See page 2-2 section 2.3 and note that multimedia instructions exist which would be executed my multimedia execution units. Consequently, the bus interfaces with media access controller devices.

24. Referring to claim 5, Intel has taught a method as described in claim 1. Intel has further taught that the data represents hexadecimal mask values 0 to 0x3FF. From page 7-165, the shifted data is a 64-bit number that may take on any of the values in the 64-bit range. Since 0-3FF is in the 64-bit range, the data may be a value from 0-3FF.

25. Referring to claim 6, Intel has taught a method as described in claim 1. Intel has further taught that the processing thread represents processing in a micro engine of a multithreaded processor. Again, see page 2-3, section 2.4.

26. Referring to claim 8, Intel has taught a method as described in claim 1. Intel has further taught that receiving the data further comprises receiving a token. See columns 91-92 and note that receiving the data to be written to the register must be preceded by receiving the shift instruction (token) itself. Therefore, the receiving of the data is coupled with receiving the token.

27. Referring to claim 9, Intel has taught a method as described in claim 8. Intel has further taught that the token represents overriding qualifiers. The shift amount is an overriding qualifier because if is the first thing that is performed in the operation (shifting and then storing). Consequently, shifting is the most important feature. Furthermore, a qualifying predicate (qp) is also a overriding qualifier as it will override the decision to execute the instruction and result in the non-execution.

28. Referring to claims 20-25 and 27-28, claims 20-25 and 27-28 are rejected for the same reasons set forth in the rejection of claims 1-6 and 8-9, respectively, because Intel has taught instructions stored on a medium for performing the method of claims 1-6 and 8-9.

Claim Rejections - 35 USC § 103

29. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

30. Claims 11-19 and 30-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen, as applied above.

31. Referring to claim 11, Nguyen has taught a method as described in claim 10. Nguyen has further taught that a token format comprises data in bits 31:0. Nguyen has not explicitly taught that the data in bit 31 corresponds to an OV field, the data in bits 30:28 corresponds to a micro engine (UENG) ADDR field, the data in bits 27:16 corresponds to a reserved field, the data in bit 15 corresponds to an OV field, the data in bits 14:5 corresponds to a fast write data field, the data in bits 4:3 corresponds to a reserved field, the data in bit 2 corresponds to an OV field, and the data in bits 1:0 corresponds to a CTX field. However, these differences are only found in the nonfunctional descriptive material as the dividing up of the token bits into named fields does not affect how the token data is used to control the system. For instance, bit 31 of the VCHGCR instruction has a meaning in the system whether or not it is called an OV field or not. Thus, the descriptive material will not distinguish the claimed invention from the prior art in terms of

patentability. See In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983); In re Lowry, 32 F.3d 1579, 32, USPQ2d 1031 (Fed. Cir. 1994). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to call a bit or any group of bits in the token a particular type of field as it does not alter how the data controls the system.

32. Referring to claim 12, Nguyen has taught a method as described in claim 11. Nguyen has further taught that a micro engine address overrides a default micro engine address if bit 31 is set. See columns 91-92 and note that the VCHGCR instruction requires that bit 31 is set. When it is set and the VCHGCR instruction executes, bits 1:0 (address of the data to control the CBANK bit) will override the CBANK bit (which is bit address). For instance, if the CBANK bit is defaulted to 1, then if bits 1:0 of the instruction are 01, then the CBANK bit will be overridden such that contains zero.

33. Referring to claim 13, Nguyen has taught a method as described in claim 11. Nguyen has further taught that bits 30:28 specify a micro engine associated with a control and status register (CSR). All of the bits of the token specify a control and status register (and consequently, the engine in which the register exists). Therefore, bits 30:28 do such specification. Without these bits, the instruction would be invalid.

34. Referring to claim 14, Nguyen has taught a method as described in claim 11. Nguyen has further taught that bits 27:16 return 0 when read. That is, if bits 27:16 are all set to 0, then when read, the value 0 would be obtained.

35. Referring to claim 15, Nguyen has taught a method as described in claim 11. Nguyen has further taught that a micro engine address overrides a default micro engine address if bit 15 is

set. See columns 91-92 and note that the VCHGCR instruction's bit 15 is an undefined bit. That is, it could equal 0 or 1 and operate the same. Consequently, when bit 15 is set and VCHGCR instruction executes, bits 1:0 (address of the data to control the CBANK bit) will override the CBANK bit (which is bit address). For instance, if the CBANK bit is defaulted to 1, then if bits 1:0 of the instruction are 01, then the CBANK bit will be overridden such that contains zero.

36. Referring to claim 16, Nguyen has taught a method as described in claim 11. Nguyen has further taught that bits 5:0 represent valid data to be written to a control and status register (CSR). That is, based on the values of these bits, certain data will be written to the CSR. Nguyen has not taught that bits 14:5 represent valid data to be written to a control and status register (CSR). However, as shown in In re Rose, 105 USPQ 237 (CCPA 1955), changes in size/range are generally not given patentable weight or would have been an obvious improvement. In this case, both applicant and the prior art teach representing data to be written to a CSR. Applicant not only represents more bits, but represents bits from a different portion of the token than the prior art. The examiner asserts that this is merely a design choice and is not given patentable weight. For instance, a person of ordinary skill in the art at the time of the invention would realized that if there are more bits in a CSR in system A than in a CSR in system B, then more data needs to be written to it. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Nguyen such that bits 14:5 represent valid data for writing to a CSR.

37. Referring to claim 17, Nguyen has taught a method as described in claim 11. Nguyen has further taught that bits 4:3 return 0 when read. That is, if bits 4:3 are all set to 0, then when read, the value 0 would be obtained.

38. Referring to claim 18, Nguyen has taught a method as described in claim 11. Nguyen has further taught that a context (CTX) field overrides a default context is bit 2 is set. From columns 91-92, if bit 2 is set, the current SMM bit operation is changed from whatever it currently is to either clear or toggle operation.

39. Referring to claim 19, Nguyen has taught a method as described in claim 11. Nguyen has further taught that bits 1:0 specify a context associated with a control and status register (CSR) reference. From columns 91-92, if bits 1:0 specify the context in which the CBANK bit is modified.

40. Referring to claims 30-38, claims 30-38 are rejected for the same reasons set forth in the rejection of claims 11-19, respectively, because Nguyen has taught instructions stored on a medium for performing the method of claims 11-19.

41. Claims 10-19 and 29-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel as applied above.

42. Referring to claim 10, Intel has taught a method as described in claim 8. Intel has further taught that the token is a 40-bit word. See page C-4, instruction I7 (shift left instruction). Intel has not taught that the token is a 32-bit word. However, as shown in In re Rose, 105 USPQ 237 (CCPA 1955), changes in size/range are generally not given patentable weight or would have been an obvious improvement. The examiner asserts that this is merely a design choice and is not given patentable weight. An instruction may be all different sizes depending on the architecture on which it is to execute. As a result, it would have been obvious to one of ordinary

skill in the art at the time of the invention to modify Nguyen such that the shift left token is 32-bits.

43. Referring to claim 11, Intel has taught a method as described in claim 10. Intel has further taught that a token format comprises data in bits 31:0. See page C-4 (instruction I7). Intel has not explicitly taught that the data in bit 31 corresponds to an OV field, the data in bits 30:28 corresponds to a micro engine (UENG) ADDR field, the data in bits 27:16 corresponds to a reserved field, the data in bit 15 corresponds to an OV field, the data in bits 14:5 corresponds to a fast write data field, the data in bits 4:3 corresponds to a reserved field, the data in bit 2 corresponds to an OV field, and the data in bits 1:0 corresponds to a CTX field. However, these differences are only found in the nonfunctional descriptive material as the dividing up of the token bits into named fields does not affect how the token data is used to control the system. For instance, bit 31 of the VCHGCR instruction has a meaning in the system whether or not it is called an OV field or not. Thus, the descriptive material will not distinguish the claimed invention from the prior art in terms of patentability. See In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983); In re Lowry, 32 F.3d 1579, 32, USPQ2d 1031 (Fed. Cir. 1994). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to call a bit or any group of bits in the token a particular type of field as it does not alter how the data controls the system.

44. Referring to claim 12, Intel has taught a method as described in claim 11. Intel has further taught that a micro engine address overrides a default micro engine address if bit 31 is clear. See page C-23 (C.3.1.7) and note that when bit 31 is 0 and a shift left occurs, data from one engine address (register) is shifted and used to override data at another engine address

(another register). Intel has not taught that such action occurs when bit 31 is set. However, the examiner asserts that this is an obvious design choice modification. The instruction would work just as well if bit 31 was set and no other instructions conflicted with it. As a result, since the functionality of applicant's claimed invention and the prior art are already the same, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify bit 31 of the token to be set.

45. Referring to claim 13, Intel has taught a method as described in claim 11. Intel has further taught that bits 30:28 specify a micro engine associated with a control and status register (CSR). All of the bits of the token specify a control and status register (and consequently, the engine in which the register exists). Therefore, bits 30:28 do such specification. Without these bits, the instruction would be invalid.

46. Referring to claim 14, Intel has taught a method as described in claim 11. Intel has further taught that bits 27:16 return 0 when read. That is, if bits 27:16 are all set to 0, then when read, the value 0 would be obtained.

47. Referring to claim 15, Intel has taught a method as described in claim 11. Intel has further taught that a micro engine address overrides a default micro engine address if bit 15 is set. See page C-4 and note that if bit 15 is set (which it may be as it's part the source register field, then the default register (destination register with current value) will be overridden with a new register address (source register which supplies the shifted data).

48. Referring to claim 16, Intel has taught a method as described in claim 11. Intel has further taught that bits 26:13 represent valid data to be written to a control and status register (CSR). See page C-4 (I7). That is, based on the values of these bits, certain data will be written

to the CSR. Intel has not taught that bits 14:5 represent valid data to be written to a control and status register (CSR). However, as shown in In re Rose, 105 USPQ 237 (CCPA 1955), changes in size/range are generally not given patentable weight or would have been an obvious improvement. In this case, both applicant and the prior art teach representing data to be written to a CSR. Applicant not only represents less bits, but represents bits from a different portion of the token than the prior art. The examiner asserts that this is merely a design choice and is not given patentable weight. For instance, a person of ordinary skill in the art at the time of the invention would realized that if there are less bits in a CSR in system A than in a CSR in system B, then less data needs to be written to it. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Nguyen such that bits 14:5 represent valid data for writing to a CSR.

49. Referring to claim 17, Intel has taught a method as described in claim 11. Intel has further taught that bits 4:3 return 0 when read. That is, if bits 4:3 are all set to 0, then when read, the value 0 would be obtained.

50. Referring to claim 18, Intel has taught a method as described in claim 11. Intel has further taught that a context (CTX) field overrides a default context is bit 2 is set. See page C-4 and note that if bit 2 is set, a certain qualifying predicate register is addressed. If the qualifying predicate is set to 0, then the instruction will not be executed, when the default is to execute anything that is selected for execution.

51. Referring to claim 19, Intel has taught a method as described in claim 11. Intel has further taught that bits 1:0 specify a context associated with a control and status register (CSR) reference. See page C-4 and note that the values of bits 1:0 will specify a certain qualifying

predicate register. If the qualifying predicate is set to 0, then the instruction will not be executed, when the default is to execute anything that is selected for execution.

52. Referring to claims 29-38, 29-38 are rejected for the same reasons set forth in the rejection of claims 7 and 10-19, respectively, because Intel has taught instructions stored on a medium for performing the method of claims 7 and 10-19.

53. Claims 7 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel as applied above, in view of Torrey et al., U.S. Patent No. 6,145,123 (herein referred to as Torrey) .

54. Referring to claim 7, Intel has taught a method as described in claim 1. Intel has further taught that loading the data comprises:

a) shifting a first portion (the entire data) of the data by an amount equal to the processing thread number. See page 7-165 and note that data is shifted left by the thread number (shift amount).

b) Intel has taught shifting a second portion of the data into bits. See page 7-165 and note the shifted data is stored in the entire destination register including bits 0-2. Intel has not taught that the bits correspond to a breakpoint register 2 through a breakpoint register 0. However, Torrey has taught the concept of writing to a breakpoint control register in order to control multiple breakpoint registers. See Fig.4 and column 8, lines 12-17. Having these bits allows for the enabling of certain breakpoint registers, which are helpful in debugging. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to have the stored bits correspond to breakpoint registers.

55. Referring to claim 26, Intel has taught a computer program product as described in claim 20. Furthermore, claim 26 is rejected for the same reasons set forth in the rejection of claim 7

above, because Intel has taught instructions stored on a medium for performing the method of claim 7.

Response to Arguments

56. Applicant's arguments filed on December 2, 2005, have been fully considered but they are not persuasive.

57. Applicant argues the novelty/rejection of claim 1 on pages 14-15 of the remarks, in substance that:

> "Nowhere, however, does Nguyen disclose that any bits of the VCSR register correspond to particular threads. Therefore, Nguyen neither discloses nor suggests loading data, using the VCHGCR instruction or otherwise, to selected bits according to a processing thread number, as required by applicant's independent claim 1."
>
> "However, nowhere does Intel disclose that data is loaded into selected bits of any register according to a processing thread number."

58. These arguments are not found persuasive for the following reasons:

a) Regarding the first argument, every instruction causes some action to occur according to a processing thread number. If thread 1 wants specific data to be loaded into a register, then data is loaded into a register according to thread 1 (thread 1 determines the data to be written). Likewise, if thread 5 wants specific data to be loaded into a register, then that data is loaded according to thread 5 (thread 5 determines everything).

b) Regarding the second argument, the examiner asserts that applicant is reading the claim too narrowly. Applicant has not defined what a thread number is within the claims. Therefore, a thread number could simply be any number associated with a thread. For instance, in Intel, the thread number is the shift amount in a thread's shift instruction. It is a number associated with a

thread. And, data is loaded by a shift instruction according to the shift amount (thread number). Applicant must further define thread number to overcome the Intel prior art.

59. Applicant argues the novelty/rejection of claim 18 on page 17 of the remarks, in substance that:

> "Bits 2-3 of the VCHGCR instruction, therefore, do not affect, in any way, the use and/or selection of context, and they certainly do not cause or affect overrides of a default context."

60. These arguments are not found persuasive for the following reasons:

a) The examiner again asserts that applicant is reading the claim, and more specifically, the word "context" too narrowly. A context is merely a setting, or a circumstance in which an event occurs (see dictionary.com, for instance). In Nguyen, a default context (default setting) could be the setting where the VCSR<SMM> bit isn't changed (bits 3:2 = 0). The system will stay in this context/setting until it is overridden by changing bits 3:2 of the instruction. For instance, if bit 2 is set, then the setting would become clear or toggle mode. Applicant needs to further clarify what is meant by context.

b) A similar argument response also applied to applicant's argument of the claim 18 Intel rejection.

61. The arguments associated with the rejections of claims 7 and 26 are moot in view of the necessitated new grounds of rejection.

Conclusion

62. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

63. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Sollars, U.S. Patent No. 5,900,025, has taught a processor having a hierarchical control register file in which a control register file exists for each thread, and a thread may include an instruction for modifying its register file (see Fig.2, Fig.16c, and claims 14-15).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
February 1, 2006

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
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